REMARKS

Claims 1-27 are currently pending in the subject application, and are presently under consideration. Claims 1-9 and 18-27 are allowed. Claims 10-17 are rejected. Claim 13 has been amended. New claims 28 and 29 have been added. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Rejection of Claim 10 Under 35 U.S.C. §103(a)

Claim 10 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,236,687 to Caso ("Caso") in view of U.S. Patent No. 6,396,804 to Odenwalder ("Odenwalder"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 10 recites a plurality of phase locked loops, each having a first block decoder configured to decode bursts of an input modulated signal at a decode rate to generate a set of associated codewords and a phase/frequency error estimate. The Office Action dated September 15, 2005, asserts that Caso discloses a demodulator unit comprising a phase locked loop having a first block decoder configured to decode bursts of an input modulated signal at a decode rate to generate a set of associated codewords and a phase/frequency error estimate (Office Action dated September 15, 2005, citing Caso, col. 3, ll. 23-35 and col. 4, ll. 9-17). Representative for Applicant respectfully disagrees with this assertion. Caso teaches a decision-directed phase-locked loop (DD-PLL) that receives an input signal, the input signal being encoded by a sequence of codewords (Caso, col. 3, ll. 23-26). The DD-PLL of Caso includes a comparator which generates a phase difference of an incoming phase of an input modulated signal and an estimated phase (Caso, col. 3, ll. 28-30). The DD-PLL taught by Caso does not generate a set of associated codewords, as recited in claim 10, because the input signal to the DD-PLL is already encoded by a sequence of codewords. Additionally, the DD-PLL taught by Caso does not generate a phase/frequency error estimate, as recited in claim 10, but merely provides a phase estimate of the quadrature pair. Furthermore, the demodulation operation recited in claim 10 is performed by a plurality of phase-locked loops, whereas Caso teaches demodulation by a single

DD-PLL. Accordingly, Caso does not teach or suggest a plurality of phase locked loops, each having a first block decoder configured to decode bursts of an input modulated signal at a decode rate to generate a set of associated codewords and a phase/frequency error estimate, as recited in claim 10.

The addition of Odenwalder does not cure the deficiencies of Caso to teach or suggest the claim elements of claim 10 as asserted in the Office Action dated September 15, 2005. Claim 10 also recites that one of the plurality of phase locked loops is adapted to selectively apply excess processing power to a burst of the input modulated signal, and that the demodulator further comprises a selection circuit which identifies a burst of the input modulated signal to be demodulated with excess processing power, the selection circuit providing the identified burst to the one of the plurality of phase locked loops which is adapted to selectively apply excess processing power in order to re-process the burst of the input modulated signal. The Office Action dated September 15, 2005 (at page 4), relies on Odenwalder to teach that one of the plurality of phase locked loops is adapted to selectively apply excess processing power to a burst of the input modulated signal. The Office Action dated September 15, 2005 (at page 4), further relies on Odenwalder to teach a selection circuit which identifies a burst of the input modulated signal to be demodulated with excess processing power, the selection circuit providing the identified burst to the one of the plurality of phase locked loops which is adapted to selectively apply excess processing power in order to re-process the burst of the input modulated signal. Odenwalder teaches a CDMA wireless communication system (Odenwalder, Abstract). The system employs decoders (BPSK and QPSK) in the CDMA receiver that employs accumulators which allow multiple decoders operating at different data rates to decode data frames at unknown data rates based on CRC checksum resultant selection (Odenwalder, col. 14, ll. 35-47). The Office Action dated September 15, 2005 (page 4), cites this section of Odenwalder to teach that one of the plurality of phase locked loops is adapted to selectively apply excess processing power to a burst of the input modulated signal. Applicant's representative respectfully asserts that such a reliance on the teachings of Odenwalder is erroneous. Odenwalder does not teach or suggest the use of a phase-locked loop, not a phase-locked loop selectively applying excess

processing power to a burst of an input modulated signal, as recited in claim 10. Furthermore, the Office Action dated September 15, 2005, equates a pilot symbol selector as taught by Odenwalder with a selection circuit which identifies a burst of the input modulated signal to be demodulated with excess processing power (Office Action dated September 15, 2005, citing Odenwalder, col. 17, ll. 34-50). The pilot symbol selector taught by Odenwalder separates control data from pilot data for separate filtering operations on each of the separate signals before delaying and recombining them through multipliers (Odenwalder, col. 17, ll. 34-50). The operation of the pilot symbol selector as taught by Odenwalder is not to identify a burst of an input modulated signal to be demodulated with excess processing power, but merely for separating a signal for filtration and subsequent recombination. Accordingly, Odenwalder does not teach or suggest a selection circuit which identifies a burst of the input modulated signal to be demodulated with excess processing power, as recited in claim 10. Therefore, neither Caso nor Odenwalder, individually or in combination, teach or suggest claim 10. Withdrawal of the rejection of claim 10, as well as claims 11-17, is respectfully requested.

II. Rejection of Claim 11-17 Under 35 U.S.C. §103(a)

Claims 11-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Caso in view of Odenwalder as applied to claim 10 above, and further in view of U.S. Patent No. 5,983,385 to Khayrallah, et al. ("Khayrallah"). Claim 13 has been amended to correct a typographical error. Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claims 11-17 depend from claim 10. For the reasons described above, claim 10 is patentable over Caso in view of Odenwalder. The addition of Khayrallah does not cure the deficiencies of Caso and Odenwalder to teach or suggest a plurality of phase locked loops, each having a first block decoder configured to decode bursts of an input modulated signal at a decode rate to generate a set of associated codewords and a phase/frequency error estimate, and that one of the plurality of phase locked loops is adapted to selectively apply excess processing power to a burst of the input modulated signal, as recited in claim 10, from which claims 11-17 depend.

Accordingly, claims 11-17 should also be patentable over the cited art. Withdrawal of the rejection of claims 11-17 is respectfully requested.

III. New Claims 28 and 29

New claims 28 and 29 have been added. Claim 28, which depends from claim 10, recites that the first block decoder of said one of said plurality of phase locked loops is configured to decode a set of vector pairs of the burst of said input modulated signal at a decode rate to generate the set of associated codewords and the phase/frequency error estimate. None of the cited art, individually or in combination, teaches or suggests the elements of claim 28. Accordingly, claim 28 should be patentable over the cited art.

New claim 29, which also depends from claim 10, recites a second block decoder that receives the phase/frequency estimates from the plurality of phase locked loops, and wherein the selection circuit identifies the burst of the input modulated signal to be demodulated with excess processing power based on the decoding operation of the second block decoder, such that the burst of the input modulated signal to be demodulated with excess processing power is re-processed by said one of said plurality of phase locked loops. None of the cited art, individually or in combination, teaches or suggests the elements of claim 29. Accordingly, claim 29 should be patentable over the cited art.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,

Date 10/17/05

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